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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/727,188	11/30/2000	Clinton M. Ramsey	10002450.1	5608
22879	7590	05/03/2004		
			EXAMINER	
			PALADINI, ALBERT WILLIAM	
			ART UNIT	PAPER NUMBER
			2125	

DATE MAILED: 05/03/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

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Office Action Summary	Application No.	Applicant(s)
	09/727,188	RAMSEY, CLINTON M.
	Examiner	Art Unit
	Albert W Paladini	2125

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) Responsive to communication(s) filed on 30 November 2000.

2a) This action is FINAL. 2b) This action is non-final.

3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) Claim(s) 1-20 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5) Claim(s) _____ is/are allowed.

6) Claim(s) 1-20 is/are rejected.

7) Claim(s) _____ is/are objected to.

8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) The specification is objected to by the Examiner.

10) The drawing(s) filed on _____ is/are: a) accepted or b) objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a) All b) Some * c) None of:

1. Certified copies of the priority documents have been received.
2. Certified copies of the priority documents have been received in Application No. _____.
3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) Notice of References Cited (PTO-892)

2) Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date 4.

4) Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____.

5) Notice of Informal Patent Application (PTO-152)

6) Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter, which the applicant regards as his invention.

2. Claims 1-20 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 1

Lines 5-6 recite, "simulating operation of said circuit utilizing said plurality of input test cases; tabulating numbers of times that each input test case stimulates logic events." It is not clear if the "logic events" recited in line 6 are the same "logic events" recited in line 2. If they are in fact the same "logic events," then it is not clear why the "simulation operation of said circuit" would stimulate the logic event, because line 2 recites "a set of logic events associated with said circuit." The phrase "associated with" does not imply a causal, one-way relationship between the circuit operation and the "logic events."

Claim 11

Lines 5-6 recite, ""a second software routine applying said plurality of input test case stimulates logic events." It is not clear if the "logic events" recited in line 6 are the same "logic events" recited in line 2. If they are in fact the same "logic events," then it is

not clear why the "simulation operation of said circuit" would stimulate the logic event, because line 2 recites "a set of logic events associated with said circuit." The phrase "associated with" does not imply a causal, one-way relationship between the circuit operation and the "logic events."

Claim 19

Lines 7-8 recite "means for tabulating numbers of times that each input test case stimulates logic events." It is not clear if the "logic events" recited in lines 7-8 are the same "logic events" recited in line 3. If they are in fact the same "logic events," then it is not clear why the "simulation operation of said circuit" would stimulate the logic event, because line 3 recites "a set of logic events associated with said circuit." The phrase "associated with" does not imply a causal, one-way relationship between the circuit operation and the "logic events."

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. Claims 1-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Weir (5729554) in view of Coburn (6618856).

This rejection is made to the extent that the claims are understood.

Art Unit: 2125

Weir discloses a computer based test system to simulate operation of a circuit using a random pattern test generator. He states in column 1, lines 6-12 "The present invention relates generally to random test generation for testing the operation of an integrated circuit design, and more particularly, to a system and method for improving the ability of a random test generator to produce effective cases by speculatively executing a test pattern to see if the events created by the test pattern are useful or whether a different test pattern should be created instead." He improves the effectiveness of the random test generator as explained in column 2 line 66 to column 3 line 15 where he states "In accordance with a preferred embodiment of the invention, there is presented an efficient method for improving the ability of a random test generator to produce effective cases by speculatively executing a test pattern. An integrated machine simulator allows a random test generator to simulate the behavior of a test pattern that it generates. After simulation, the machine state may be inspected to determine if the test pattern contributed to the usefulness of the case. If it did, then the test pattern is saved and the process repeats for generation of subsequent test patterns until enough patterns have been created. The number of test patterns in a case is controlled by the user of a random test generator. However, if after simulation and inspection of the resulting machine state it is determined that a test pattern does not provide useful testing, the test pattern is discarded and the machine state is reset to its previous state and a different test pattern is produced." Occurrences and non-occurrences of events are considered in column 7 lines 16-29 where Weir states, "The utility of the present invention may also be helpful in controlling the rate at which certain events occur. For example, if a test pattern is a branch instruction, information about the branch can be analyzed, including whether the branch was taken and whether it branched forward or backward. The branch test pattern may be accepted or rejected to provide a test case containing an equal number of taken and not-taken branches or so that an equal number of forward and backward branches occur. As another example, a test pattern can be analyzed to see if it caused an interruption to the normal processing of instructions. The random test generator may control the rate at which interruptions occur by rejecting test patterns that either cause too many or too few interruptions." Although the taken and non-taken branches imply the identification of logic events that have not been stimulated as recited in claims 1, 11, 19; Weir does not explicitly describe non-stimulated logic events.

Coburn (6618856) discloses a simulation method and apparatus and provides the motivation and method for identifying non-occurring logic events in column 14 lines 42-52 where he states "In addition to the inventive aspects described above, in another aspect the invention includes status based diagnostics wherein every event which is to occur during a process is monitored and, when an expected event fails to occur, the failed event is reported. For example, where a clamp extension request is contingent upon the occurrence of ten previous events, when one of the previous events fails, status based diagnostics reports the failed event. In this manner, when a failure occurs, the specific symptoms of the failure are immediately reported and the operator can then surmise the cause of the failure quickly."

In order for the operator to quickly to the occurrence of a failure in a circuit being stimulated by a random test pattern, it would have been obvious to one of ordinary skill in the art to combine the teachings of Weir and Coburn.

Relevant Prior Art

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Suzuki (5404360) discloses a simulator for simulating the operation of a logic circuit where a storage area contains information such as the output value of the device when the signal is changed upon occurrence of an event in each device and its time, terminal information as to which input terminal of the simulated circuit was supplied with the test pattern which caused the change in the output, and the signal value of the test pattern causing the error and its time.

Yemini (6249755) discloses a computer system with the methods and means for detecting the occurrence of exceptional events in a complex system and identifying which particular event occurred and where it occurred. The set of events which occur are detected in the system over a period of time will be referred to as an "event stream." The system does not consider the location of the event as the location where it is observed, because events can propagate across related entities in a system. Although every possible reportable measurement (such as voltage level, disk error, or temperature level) could be considered to be an "event", many of these measurements do not contribute to identifying exceptional events in the system. Event correlation takes as input an event stream, detects occurrence of exceptional events, identifies the particular events that have occurred, and reports them as an output.

6. Any inquiry concerning this communication or earlier communication from the examiner should be direct to Albert W. Paladini whose telephone number is (703) 308-2005. The examiner can normally be reached from 7:30 to 3:30 PM on Monday, Tuesday, Thursday, and Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mr. Leo P. Picard, can be reached on (703) 308-0538. The official fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

April 26, 2004

Albert W. Paladini
Albert W. Paladini
Primary Examiner
Art Unit 2125